Available online at www.sciencedirect.com
ScienceDirect
Int. J. Electron. Commun. (AEÜ) 61 (2007) 300–306
International Journal AEÜ of Electronics and Communications
www.elsevier.de/aeue

On the realization of electronically current-tunable CMOS OTA

Khanittha Kaewdang*, Wanlop Surakampontorn

Faculty of Engineering and Research Center for Communication and Information Technology (ReCCIT), King Mongkut's Institute of Technology Ladkrabang (KMITL), Ladkrabang, Bangkok 10520, Thailand

Received 2 September 2005

Abstract

A CMOS operational transconductance amplifier (OTA) called as an EOTA, where its transconductance gain can be electronically and linearly tuned is proposed in this paper. The realization method is achieved by squaring the transconductance gain of the balanced CMOS OTA. The EOTA transconductance gain can be linearly tuned by an external bias current for three decades. The linear input-voltage range of about 1 Vp with less than 1% nonlinearity is obtained. The usefulness of the proposed EOTA is demonstrated through application example with a current multiplier. The performance of the proposed circuit is discussed and confirmed through PSPICE-simulation results.

Keywords: CMOS OTA; Electronically and linearly tuned; Current controlled

1. Introduction

Linear transconductors or voltage-to-current converter circuits are fundamental building blocks of analog circuits and systems. They are found useful in interface circuits, instrumentation amplifiers, continuous-time-filters and oscillators. In addition, when the transconductance gain of the transconductor can be electronically varied, they can also be applied in automatic gain control circuits and in analog multipliers. In the last two decades, it is well accepted that a linear transconductor, which is constructed from a bi-polar differential pair and current mirrors, called as an operational transconductance amplifier (OTA), is one of the essential active building blocks in the design of analog circuits [1–3]. This is due to the fact that the OTA is a low-cost device that has only a single high-impedance node and its transconductance gain g_m can be linearly controlled over more than four decades by means of an external bias current. Moreover, the implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplified the design.

In CMOS technology, several linearly tunable transconductors based on the use of MOS transistors operating in saturation region have been proposed in the literature [4–7]. Most of them are functioning in voltage-controlled mode. The method of source-follower of Ref. [4] is operated in square law characteristic with constant source-bulk voltages, where the control voltage is applied to the gate. Whereas for the cross-coupled connection methods [5–7], the transconductance control voltages are applied through voltage-level shifters. However, their controllable voltage ranges are rather limited and only narrow linearly tunable transconductance ranges are available. In some applications, such as, an analog multiplier circuit, a frequency divider/multiplier circuit and an arbitrary power-law circuit, current-controlled transconductors that this transconductance gain can be linearly controllable by a DC bias current are preferable [8–10]. In the past, a current-controlled CMOS transconductor was

* Corresponding author.
E-mail address: s5160306@kmitl.ac.th (K. Kaewdang).

1434-8411/$ - see front matter © 2006 Elsevier GmbH. All rights reserved.
doi:10.1016/j.aeue.2006.05.011

presented in Ref. [11]. But the linearly tunable transconductance range is narrow due to the MOS transistors are working in the weak-inversion region.

The main objective of this paper is, therefore, to present a circuit design technique for the synthesis of a linear electronically tunable CMOS OTA, called as an EOTA. Since, the realization method is achieved by squaring the transconductance gain of the CMOS OTA, the transconductance gain of the EOTA is directly depend on the DC bias current. To provide a maximum output voltage swing and wide linearly tunable transconductance range, a balanced CMOS OTA or voltage-to-current transducer will be employed as basic active circuit elements to realize the EOTA, whereas the completed EOTA requires three balanced CMOS OTA's. Since it is generally assumed that all MOS transistors are operating in the saturation region, the individual functions of the circuits are derived from the approximate square-law characteristic of MOS transistors in saturation. In addition, it is well accepted that the design and implementation of electronically tunable analog circuits using bipolar-based OTA as active circuit elements are well established and well tabulated. Then, having access to such a linear electronically tunable CMOS OTA, it would enable us to realize CMOS analog circuits with their property can be electronically tuned by simply replacing a bipolar OTA with an EOTA. This kind of advantage will be demonstrated through an application example. The proposed EOTA is employed to implement a current multiplier circuit, that using only active elements and without the requirement of external passive elements. The circuit performances are studied through PSPICE-simulation results.

2. Circuit description

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. This means that the transistor drain current I_D is characterized by a square-law model as

$$I_D = K(V_{GS} - V_T)^2 \quad \text{for } V_{GS} > V_T,$$
$$= 0 \quad \text{for } V_{GS} \leqslant V_T, \tag{1}$$

where the transconductance parameter $K = \mu C_{ox} W/2L$, μ is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and the threshold voltages, respectively.

2.1. A balanced CMOS OTA

Fig. 1 shows a balanced single-output CMOS OTA, which is formed by MOS coupled pair and current mirrors, where V_{in} is the differential input voltage ($V_{in} = V_1 - V_2$), i_o is the output current and I_{BB} is the bias current. Let us assume that M_1 and M_2 are perfectly matched and the current mirrors

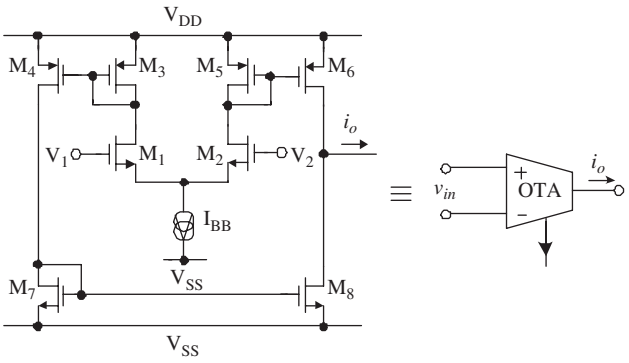

Fig. 1. Schematic diagram of a balanced CMOS OTA.

have unity current gain. By using Eq. (1), the differential output current of the circuit in Fig. 1 can be given by [12]

$$i_o = i_2 - i_1$$
$$= \sqrt{2I_{BB}K}\, V_{in}\sqrt{1 - \frac{KV_{in}^2}{2I_{BB}}} \quad \text{for}$$
$$-\sqrt{\frac{I_{BB}}{K}} \leqslant V_{in} \leqslant \sqrt{\frac{I_{BB}}{K}}. \tag{2}$$

The transconductance gain (g_m) of the fully differential OTA can be derived by taking the derivative of Eq. (2) with respect to V_{in}, yielding

$$g_m = \left.\frac{di_o}{dV_{in}}\right|_{V_{in}=0}$$
$$= \sqrt{2I_{BB}K} \quad \text{for}$$
$$-\sqrt{\frac{I_{BB}}{K}} \leqslant V_{in} \leqslant \sqrt{\frac{I_{BB}}{K}}. \tag{3}$$

From Eq. (2), the current i_o can written as

$$i_o = g_m V_{in} = \sqrt{2I_{BB}K}\, V_{in}. \tag{4}$$

Eq. (3) shows that the transconductance gain (g_m) of the OTA can be varied by the bias current I_{BB}, but in the form of square root function. In addition, in order to operate in the low distortion range, where all the transistors are operated in saturation, the input voltage V_{in} should be in the range of [13]

$$V_{in} \leqslant \left|\sqrt{I_{BB}/K}\right|. \tag{5}$$

2.2. The proposed electronically and linearly tunable CMOS OTA

Through the use of three balanced single-output CMOS OTAs, a CMOS-based electronically and linearly tunable OTA, called as an EOTA, can be realized by the circuit diagram shown in Fig. 2. The OTA_1 converts a differential input signal voltage $v_{in} = v_1 - v_2$ into a signal current i_L to

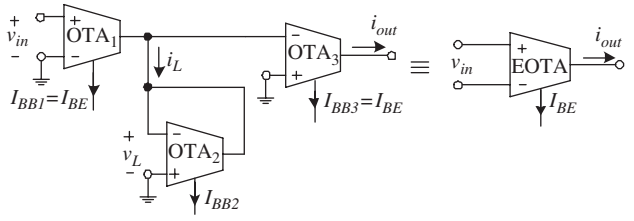

Fig. 2. The proposed EOTA.

flow into an active resistor R_L, formed by the OTA_2, where $Z_L = 1/g_{m2}$ and g_{m2} represents the transconductance gain of the OTA2. Since the current signal $i_L = g_{m1}v_{in}$, the voltage drop across the active resistor (OTA_2) becomes

$$v_L = i_L z_L = g_{m1} v_{in} \frac{1}{g_{m2}}. \tag{6}$$

The OTA_3 will convert the voltage v_L, with the transconductance gain of g_{m3}, into the output current i_{out} as

$$i_{out} = g_{m3} v_L = g_{m1} v_{in} \frac{1}{g_{m2}}. \tag{7}$$

From Eqs. (6) and (7), the current i_{out} can be rewritten as

$$i_{out} = \frac{g_{m1} g_{m3}}{g_{m2}} v_{in}. \tag{8}$$

Since $g_{m1} = \sqrt{2I_{BB1}K_1}$, $g_{m2} = \sqrt{2I_{BB2}K_2}$ and $g_{m3} = \sqrt{2I_{BB3}K_3}$, if we set $I_{BB1} = I_{BB3} = I_{BE}$, then from Eq. (8), we obtain

$$i_{out} = \frac{2I_{BE}\sqrt{K_1 K_3}}{\sqrt{2I_{BB2}K_2}} v_{in} = g_{mT} v_{in}, \tag{9}$$

where g_{mT} represents the transconductance gain of the proposed EOTA and can be expressed as

$$g_{mT} = 2I_{BE}K_T \tag{10}$$

and $K_T = \sqrt{K_1 K_3 / 2I_{BB2}K_2}$, which can usually be kept at constant. Eq. (10) clearly indicted that the transconductance gain of the proposed EOTA can be electronically and linearly tuned by the bias current I_{BE}. This linear relationship is in the form that similar to the transconductance gain of the bi-polar-based OTA that found useful in many applications [14]. Since the balanced CMOS OTA is formed by MOS coupled pair and current mirrors, therefore, the proposed EOTA is very suitable for fabricating in CMOS integrated form.

3. Performance of the EOTA

It is well accepted that the prediction of Eq. (10) will be valid only for a small value of V_{in}. From Eq. (5), since OTA_1 and OTA_3 are formed by MOS coupled pairs, to maintain in the linear range and low total harmonic distortion, the voltages V_{in} and V_L should, respectively, be restricted to the ranges of [13]

$$|V_L|_{MAX} = 0.4/\sqrt{2}K\ Z_L$$

and

$$|V_{in}|_{MAX} = 0.4\sqrt{I_{BB}/K}, \tag{11}$$

where it should be noted from Eq. (11) that the maximum usable voltage range is limited by $|V_L|_{MAX}$ if $g_{m1}/g_{m2} > 1$ and it is limited by $|V_{in}|_{MAX}$ if $g_{m1}/g_{m2} < 1$. For example, for $I_{BE} = 1$ mA and $I_{BB2} = 700$ μA, the maximum usable range is determined by $|V_L|_{MAX}$ and $|V_L|_{MAX}$ is about 0.94 V, for $K = \mu_n C_{ox} W/2L = 1.27 \times 10^{-4}$ A/V^2, $\mu_n C_{ox} = 5.08 \times 10^{-5}$ V and $W/2L = 2.5$.

The transconductance gain error that results from in the inaccuracy of the EOTA can be determined from a large signal analysis. Consider the balanced CMOS OTA, the transconductance gain G_m of the Eq. (2) can be written as

$$G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_{BB}K}\sqrt{1 - \frac{KV_{in}^2}{2I_{BB}}} \quad \text{for} \quad -\sqrt{\frac{I_{BB}}{K}} \leqslant V_{in} \leqslant \sqrt{\frac{I_{BB}}{K}}. \tag{12}$$

If we set the transconductance error of the balanced CMOS OTA of Fig. 1 as $E = KV_{in}^2/2I_{BB}$, then Eq. (12) can be rewritten as

$$G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_{BB}K}\sqrt{1 - E}. \tag{13}$$

We found that the G_m will equal to the g_m of Eq. (3) in the condition that $KV_{in}^2/2I_{BB} \ll 1$. This can be achieved by keeping the input voltage signal V_{in} small or set the DC bias current I_{BB} to a large value.

By applying the G_m of Eq. (13) to the circuit of Fig. 2, we obtain the transconductance gain of the proposed EOTA for large signal as

$$G_{mT} = 2I_{BB}K_T\left(1 + \frac{\sqrt{1-E_1}\sqrt{1-E_3} - \sqrt{1-E_2}}{\sqrt{1-E_2}}\right), \tag{14}$$

where the errors $E_1 = K_1 V_{in1}^2/2I_{BB1}$, $E_2 = K_2 V_{in2}^2/2I_{BB2}$ and $E_3 = K_3 V_{in3}^2/2I_{BB3}$ are the transconductance errors due to the OTA_1, OTA_2 and OTA_3, respectively. Given that E_T is the transconductance error of the EOTA from the linear transconductance gain, we can write

$$E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3} - \sqrt{1-E_2}}{\sqrt{1-E_2}}. \tag{15}$$

Thus, we have the percent of the conversion error as

$$\%\ E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3} - \sqrt{1-E_2}}{\sqrt{1-E_2}} \times 100\%. \tag{16}$$

For example, if $V_{in1}=0.5$ V, $V_{in2}=V_{in3}=0.751$ V, $I_{BB1}=I_{BB3}=I_{BE}=1$ mA, $I_{BB2}=700$ μA and $K_1=K_2=K_3=1.27\times 10^{-4}$ A/V^2, the resulting transconductance error (% E_T) is equal to 0.54%.

4. A current multiplier circuit

In order to demonstrate the applications and the usefulness of the proposed EOTA, an application example will be outlined in this section. It outlines the use of the EOTA to realize the current-mode multiplier which employs only active circuit elements.

The current multiplier circuit is shown in Fig. 3. This application is adapted from the bipolar-based OTA-based circuits by replacing the bipolar-based OTA with the proposed EOTA [15]. From the figure, the input signal current i_{in1} is injected into the EOTA$_1$, which is connected as a current-controlled grounded resistor. The voltage across the EOTA$_1$ is then used as the input voltage for the EOTA$_2$ and EOTA$_3$. The input signal current i_{in2} is added with the bias current I_{B2} of the EOTA$_2$. Let g_{mT1}, g_{mT2} and g_{mT3} be the transconductance gains of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively. Then from Eq. (9) and from routine circuit analysis the output currents i_{o2} and i_{o3} of the EOTA$_2$ and EOTA$_3$, respectively, can be written as

$$i_{o2}=\frac{g_{mT2}}{g_{mT1}}i_{in1}=\frac{(I_{BE2}+i_{in2})}{I_{BE1}}i_{in1} \tag{17}$$

and

$$i_{o3}=-\frac{g_{mT3}}{g_{mT1}}i_{in1}=-\frac{I_{BE3}}{I_{BE1}}i_{in1}, \tag{18}$$

where I_{BE1}, I_{BE2} and I_{BE3} represent the DC bias current of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively, and the transconductance gains $g_{mT1}=2I_{BE1}K_{T1}$, $g_{mT2}=2(I_{BE2}+i_{in2})K_{T2}$ and $g_{mT3}=2I_{BE3}K_{T3}$. If we set $I_{BE2}=I_{BE3}=I_B$,

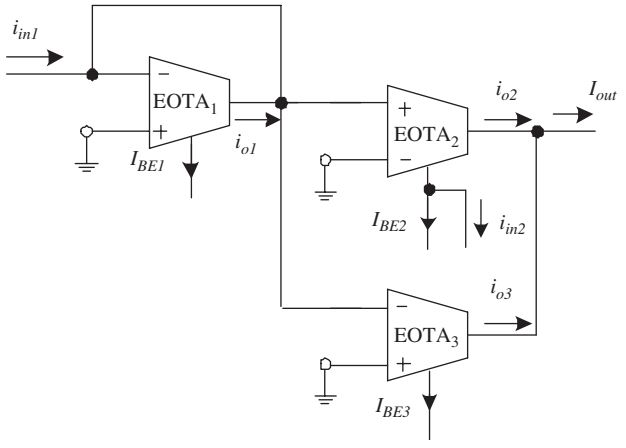

Fig. 3. The multiplier circuit using EOTA.

the output current I_{out} of the circuit that is the summation of the currents i_{o2} and i_{o3} can be expressed as

$$I_{out}=i_{o2}+i_{o3}=\frac{i_{in1}i_{in2}}{I_{BE1}}, \tag{19}$$

which is in the form of a current multiplication function.

5. Simulation results

The performance of the proposed EOTA of Fig. 2 and its applications were verified through the use of PSPICE-simulation results. All the balanced CMOS OTA was simulated by using CMOS transistor parameters of the SCN2 level 2 of MOSIS [16]. The dimensions of transistors M_1 and M_2 are $W=50$ μm and $L=10$ μm, the dimensions of the transistor M_3-M_8 are $W=100$ μm and $L=10$ μm. The power supply voltage were set to $V_{DD}=-V_{SS}=\pm 5$ V. Fig. 4 shows the simulated transfer characteristic of the EOTA of Fig. 2. The plots of the output current I_{out} versus the input voltage V_{in} show that, for the DC bias current (I_{BE}) in the cases of 1 mA, 800 μA and 400 μA, the EOTA can linearly convert the input voltage into output signal current with nonlinearity of less than 1% for the input voltage (V_{in}) in the ranges of −1 to 1 V, −0.86 to 0.86 V and −0.66 to 0.66 V, respectively. These results were agreed with the prediction value from Eq. (9). For example, for the case of the DC bias current $I_{BE}=1$ mA and for $V_{in}=0.86$ V, $I_{BB2}=700$ μA, the transconductance gain $g_{mT}=5.398\times 10^{-4}$ A/V, where the conversion error is about 0.5%. The frequency response of the EOTA was also studied, where the −3 dB bandwidth of about 120 MHz is achieved.

The plot of the relation between the transconductance gain g_{mT} and the bias current I_{BE} in Fig. 5 is measured by fixing $V_{in}=0.1$ V and varying I_{BE} from 10 nA to 1 mA. It shows that the transconductance gain g_{mT} can be linearly tuned by the bias current I_{BE} over the range of 1 μA–1 mA (three decades), where the simulated conversion error found to be about 0.68%. The similar relation of g_{mT} versus I_{BE} are also obtained for the cases of fixing $V_{in}=0.2$ V and $V_{in}=0.5$ V. But in these cases the linear tunable ranges should be started at the current I_{BE} that must more than 5 and 32 μA, respectively, since the entire MOS transistors must be operated in saturation region.

To demonstrate that the circuit of Fig. 3 can be functioned as current multiplier, two sinusoidal current signals are applied. Fig. 6 shows the response for the case of $i_{in1}=0.2\sin(2\pi 1000t)$ mA, $i_{in2}=0.2\sin(2\pi 20\,000t)$ mA and $I_{B1}=1$ mA. This result confirms that the circuit can accurately modulate two different input signal currents. The DC transfer characteristics of the multiplier circuit shown in Fig. 7 were observed by setting the bias currents $I_{B1}=I_{B2}=I_{B3}=1$ mA, and the input current i_{in1} and i_{in2} are varied from −200 μA to 200 μA with 100 μA per step. The transfer characteristic demonstrated that the simulated and calculated data are agreed very well over the input range of

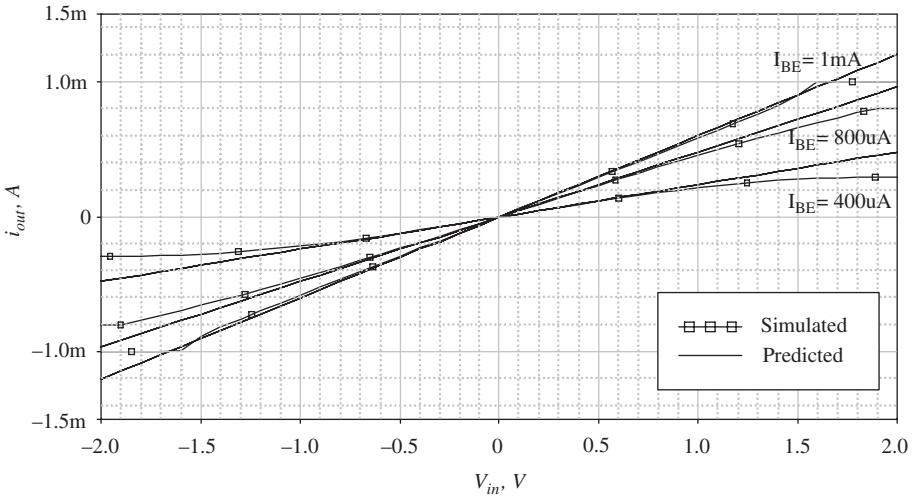

Fig. 4. DC transfer characteristics of the EOTA.

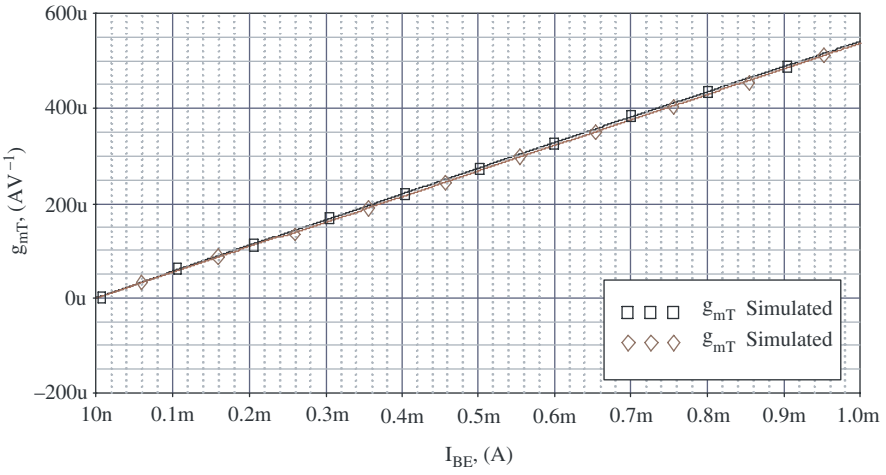

Fig. 5. Linear transconductance tunable range.

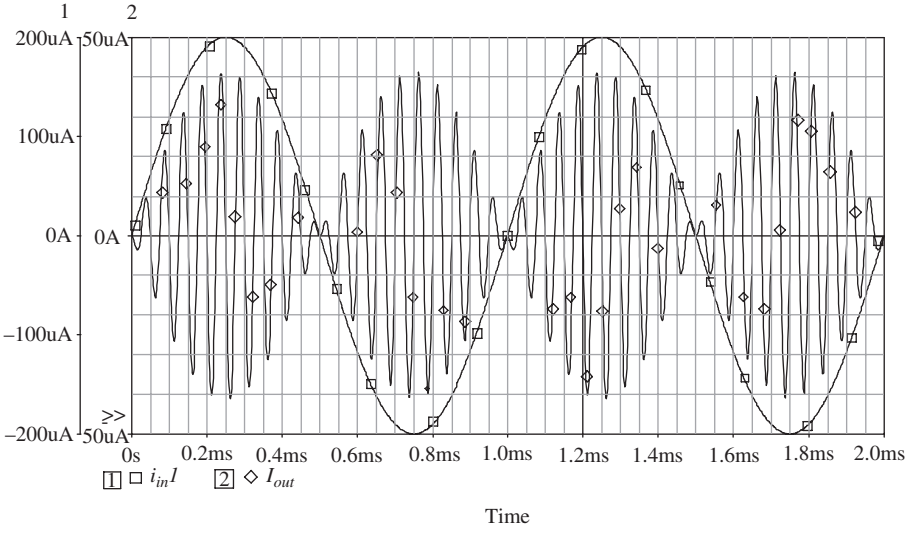

Fig. 6. Simulated transient response of the multiplier circuit.

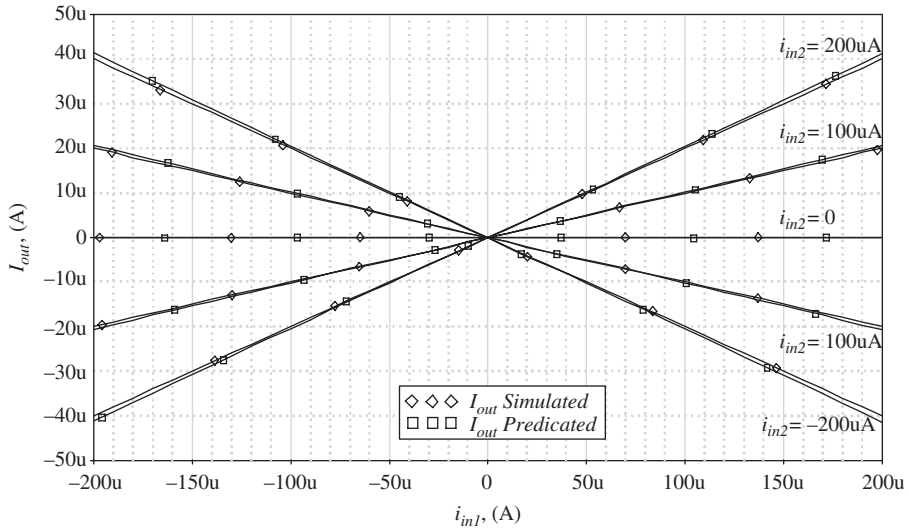

Fig. 7. Simulated DC transfer characteristic of the multiplier.

190 μA with the error of less than 1%. The high-frequency characteristic of the multiplier circuit is also studied. The simulated −3 dB bandwidth for the case of the input i_{in1} to the output I_{out}, with $i_{\text{in1}} = 0.5\sin(2\pi 10\,000t)$ mA, $i_{\text{in2}} =$ 500 μA and $I_{\text{B1}} = 1$ mA, is about 75 MHz and the simulated −3 dB bandwidth of the circuit for the input i_{in2} to the output I_{out}, with $i_{\text{in2}} = 0.5\sin(2\pi 10\,000t)$ mA, $i_{\text{in1}} = 500$ μA and $I_{\text{B1}} = 1$ mA, is about 71 MHz.

6. Conclusion

A design of the CMOS-based electronically and linearly current-tunable OTA has been proposed. The EOTA circuit composed of three balanced CMOS OTAs which is suitable for implementing in CMOS integrated form. The achieve characteristics of the proposed circuit were similar as the bipolar OTA that the transconductance gain (g_m) can be linearly tuned by the DC bias current. Simulation results have been employed to demonstrate the performances of the proposed EOTA. Moreover to confirm that EOTA can be replacing the bipolar OTA, the current-mode multiplier circuit is used to display the performances of the proposed circuit.

Acknowledgments

This work was funded by the Thailand Research Fund through the Royal Golden Jubilee Ph.D. Program (Grant No. PHD/0107/2546) to Khanittha Kaewdang and Wanlop Surakampontorn and financial support from the Thailand Research Fund (TRF) under the Senior Research Scholar Program, Grant No. RTA4680003 acknowledge these supports.

References

[1] Senani R. A simple approach of deriving single-input-multiple-output current-mode biquad filters. Electron Lett 1989;25:19–21.
[2] Chung WS, Kim KH, Cha HW. A linear operational transconductance amplifier for instrumentation applications. IEEE Trans Instrum Meas 1992;41:441–3.
[3] Iqbal Khan A, Ahmed Muslim T. Wide-range electronically tunable multifunctional OTA-C filter for instrumentation applications. IEEE Trans Instrum Meas 1987;IM-36:13–7.
[4] Klumperink E, Zwan EVD. CMOS variable transconductance circuit with constant bandwidth. Electron Lett 1989;25: 675–6.
[5] Huang S-C, Ismail M. Linear tunable COMFET transconductor. Electron Lett 1993;29:459–61.
[6] Wang Z, Guggenbuhl W. A voltage-controllable linear MOS transconductor using bias offset technique. IEEE Solid State Circuits 1990;25:315–7.
[7] Wilson G, Chan PK. Saturation-mode CMOS transconductor with enhanced tunability and low distortion. Electron Lett 1993;29:459–61.
[8] Silva-Martinez J, Sanchez-Sinencio E. Analogue OTA multiplier without input voltage swing restrictions and temperature-compensated. Electron Lett 1986;22:599–600.
[9] Tarun SK, Arabinda R, Baidyanath RN. An arbitrary power-law device based on operational transconductance amplifiers. IEEE Trans Instrum Meas 1993;42:948–52.
[10] Abuelma'atti MT. A novel analogue current-mode current-controlled frequency divider/multiplier. Int J Electron 2002;89:455–65.
[11] Hung C-C, Halonen K. Micropower CMOS GM-C filters for speech signal processing. In: IEEE International Symposium on Circuit and Systems. 1997. p. 1972–4.
[12] Surakampontorn W, Kumwachara K, Riewruja V, Surawatpunya C. CMOS-based integrable electronically tunable floating general impedance inverter. Int Electron 1997;82: 33–44.

[13] Toumazu C, Lidgey FT, Haigh DG. The current mode approach. London, UK: Peter Feregrinus; 1990.
[14] National Semiconductor. Dual operational transconductance amplifiers with linearizing diodes and buffers. General purpose linear devices databook, 1989.
[15] Kaewdang K, Fongsamut C, Surakampontorn W. A realization of biquadratic circuit using MO-CCIIs and capacitors. In: IEEE international symposium on circuit and systems Bangkok. Thailand, 2003. p. 349–54.
[16] Elwan HO, Soliman AM. Low-voltage low-power CMOS current conveyors. IEEE Trans Circuits Systems 1997;44: 828–35.

Khanittha Kaewdang was born in Sisaket, Thailand. She received her B. Eng. degree in Electrical Engineering from the Ubon Rajathanee University, Ubon Rajathanee, Thailand, in 1999 and M. Eng. degree in Electronics Engineering from the King Mongkut's Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, in 2002. She is currently working toward the Dr. Eng. degree at the KMITL. Her research interests include analog signal-processing, analog integrated circuit, and electronic instrumentation.

Wanlop Surakampontorn (S'80–M'84) was born in Bangkok, Thailand. He received his B. Eng. and M. Eng. degrees in Electrical Engineering from the King Mongkut's Institute of Technology Ladkrabang (KMILT), Bangkok, Thailand, in 1976, and 1978, respectively, and his Ph.D. in Electronics from the University of Kent at Canterbury, Kent, UK, in 1983. Since 1978, he has been a Member of the Department of Electronics, Faculty of Engineering, KMITL, where he is currently a Professor of Electronic Engineering. His research interests are in the areas of analog and digital integrated circuit designs, real-time application of PC computers and microprocessors, digital signal processing, electronic instrumentation, and VLSI signal processing.

Dr. Surakampontorn received the Outstanding Scientist of Thailand Award in 1996 and The National Award for Distinguished Researcher, Thailand, in 1998. He is a Senior Member of the IEEE and is a Member of the IEICE.