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A translinear-based true RMS-to-DC converter using only npn BJTs

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Abstract

A true rms-to-dc converter based on the explicit computation technique is proposed in this paper. Since the scheme utilizes translinear principle circuits to realize current-mode squarer, averaging and square root circuits, only npn bipolar junction transistors are required. The conversion circuit has wide-band frequency response and can be operated with single supply voltage at 2 V. PSPICE simulation and experimental results show good agreement with the theoretical predictions.

Keywords: Bipolar analog integrated circuits; Squarer circuit; Averaging circuit; Square root circuit; True RMS to DC converter

1. Introduction

A true rms-to-dc converter is a device that generates an output direct current (dc) such that its value is proportional to the average energy content in an electrical signal. This device is found useful in the fields of instrumentation, communication and display systems. Many true rms-to-dc converters are available [1–4]. However, most of these devices are similarly built up from two main parts: a full-wave rectifier (or absolute-value) circuit and a multiplier/ divider circuit employing a log–antilog principle. Due to the bandwidth and the slow rate of the full-wave rectifiers, the high-frequency performances of these devices are limited to less than 5 MHz. Design techniques based on bipolar dynamic translinear circuits have been proposed to implement true rms-to-dc converters [5,6]. Although these schemes require only npn transistors, their circuits are operated in only one quadrant and employ full-wave rectifier. Recently, a new design technique for rms-to-dc converter that designs around a dual translinear-based squarer circuit is proposed [7], where the input current can be a two-quadrant current signal. Because the full-wave rectifier is not required by this conversion scheme, the circuit exhibits a wide bandwidth. However, the implementation circuit is rather complicated, requires both the npn and the pnp transistors and suitable for a supply voltage of more than 5 V.

The purpose of this paper is to propose a translinear-based true rms-to-dc converter that can be operated at a low supply voltage. The realization scheme is through the implicit computation method [8,9]. Since the translinear-based squarer, averaging and square root circuits are employed, the conversion circuit is simple and requires only npn bipolar transistor. The rms-to-dc conversion circuit can be operated with low supply voltage, which is suitable for battery-operated portable equipment. The circuit shows a wide −3 dB bandwidth because an absolute-value circuit is not required and the circuit does not employ pnp devices. Furthermore, the

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circuit can be implemented using cheap bipolar processes rather than implemented by the more expensive BiCMOS processes or the bipolar processes featuring high-quality pnp transistors. The circuit performances are studied through PSPICE simulation and experimental results.

2. True RMS- to DC-converter

2.1. Circuit description

Fig. 1 shows the schematic diagram of a translinear-based current squaring circuit, where I_{IN} and I_{SQ} are the input and the output currents, respectively. The emitter-area of the transistors Q_4 and Q_5 are double of the emitter-area of the transistors Q_1, Q_2 and Q_3. The external bias currents I_{B1}, I_{B2} and I_{B3} of this circuit are arranged such that $I_{C2}+I_{C3}=I_{B1}$, $I_{C4}=I_{B2}$ and $I_{C5}+I_{SQ}=I_{B3}$. By applying the translinear principle to the loop formed by the transistors Q_1, Q_2, Q_4 and Q_5, if we assume that the common emitter current gain of all the transistors is much greater than unity, we obtain [10–13]

$$V_{BE1}+V_{BE2}=V_{BE4}+V_{BE5} \tag{1}$$

$$V_T\ln\left(\frac{I_{C1}}{I_{S1}}\right)+V_T\ln\left(\frac{I_{C2}}{I_{S2}}\right)=V_T\ln\left(\frac{I_{C4}}{I_{S4}}\right)+V_T\ln\left(\frac{I_{C5}}{I_{S5}}\right) \tag{2}$$

and

$$I_{C1}I_{C2}=\frac{I_{C4}}{2}\frac{I_{C5}}{2} \tag{3}$$

From Fig. 1, by neglecting the transistor base currents, we get

$$I_{C1}=I_{IN}+I_{C2}=I_{C3} \tag{4}$$

and

$$I_{C2}=I_{B1}-I_{C3} \tag{5}$$

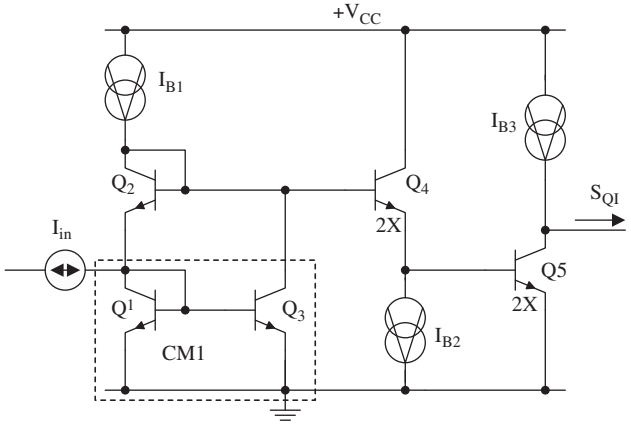

Fig. 1. Translinear current squaring circuit.

Combining Eqs. (4) and (5), we have

$$I_{C1}=\frac{I_{B1}+I_{IN}}{2} \tag{6}$$

$$I_{C2}=\frac{I_{B1}-I_{IN}}{2} \tag{7}$$

If we set the currents $I_{B1}=I_{B2}=I_{B3}=I_B$, where $I_{C4}=I_{B2}$, $I_{C5}=I_{B3}-I_{SQ}$, then by substituting Eqs. (6) and (7) into Eq. (3) and solving for I_{SQ} yields

$$I_{SQ}=\frac{I_{IN}^2}{I_B} \tag{8}$$

Note that the circuit of Fig. 1 is a two-quadrant squarer or I_{IN} can be a plus or minus value. For a good operation, the value of the input current I_{IN} should be restricted to $I_{IN}<I_B$ or $-I_B<I_{IN}<I_B$.

The completed true rms-to-dc conversion circuit that uses only npn bipolar junction transistors is shown in Fig. 2. The circuit comprises the squarer circuit of Fig. 1 and the averaging and the square rooter circuits. As indicated in Eq. (8), the current I_{IN} inputs through the squaring circuit and results in the squaring current I_{SQ}. The current I_{SQ} is passed through the first-order low-pass filter or averaging circuit, which consists of the current mirror CM_2, formed by transistors Q_6 and Q_7, with the capacitor C_{AV} connected in parallel to the input port of CM_2. The averaging current I_{AV} can be written as

$$I_{AV}=\frac{1}{I_B\tau}\int I_{IN}^2\,dt \tag{9}$$

where $\tau=C_{AV}/g_{m6}$ is the time constant of the averaging circuit, g_{m6} is the transconductance gain of the transistor Q_6. The current I_{AV} is flowed through the translinear square-rooting circuit formed by the transistors Q_8–Q_{11}. It is structured in considerably the same manner as that of Fig. 1, the loop Q_8–Q_{11} translinear operation results in expression

$$I_{C8}I_{C9}=I_{C10}I_{C11} \tag{10}$$

since $I_{C9}=I_{B4}$, $I_{C8}=I_{AV}$ and $I_{C10}=I_{C11}=I_{rms}$, the current I_{rms} can be written as

$$I_{rms}=\sqrt{\frac{I_{B4}}{I_B\tau}\int I_{IN}^2\,dt} \tag{11}$$

If we set $I_{B4}=I_{B1}=I_{B2}=I_{B3}=I_B$, we get

$$I_{rms}=\sqrt{\frac{1}{\tau}\int I_{IN}^2\,dt} \tag{12}$$

Now the output current I_{rms} is the root-mean-square value of the input current I_{IN}.

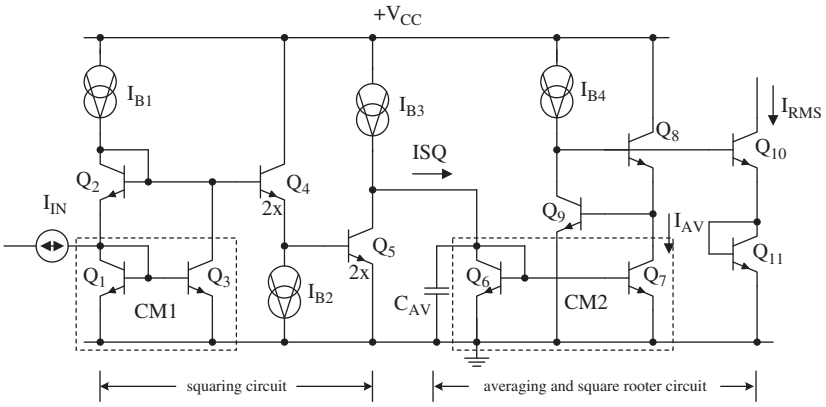

Fig. 2. Circuit diagram of the translinear-based true rms-to-dc converter using only npn BJTs.

2.2. Circuit performance

In practical circuit, not only the current I_{rms} is presented at the output, but there are also a low-frequency ripple component and a dc error. These errors depend on the value of the capacitor C_{AV} and the frequency of the input signal current I_{IN}. The errors can be computed by expressing the relationship of the currents I_{rms} and I_{IN} in the form of transfer function as [14]

$$I_{\text{OUT}} = \sqrt{\frac{I_{\text{IN}}^2}{1+s\tau}} \tag{13}$$

The current I_{IN} is a sine wave input of the form

$$I_{\text{IN}} = I_{\text{M}}\sin(\omega t) = \sqrt{2}I_{\text{rms}}\sin(\omega t) \tag{14}$$

where $\omega = 2\pi f$, f is the frequency of input current and I_{M} is the amplitude of input current. Using some simple trigonometric and Taylor series approximation and by assuming that the frequency of input current is greater than the inverse of the averaging time constant τ (or $f > 1/\tau$), the output current becomes

$$I_{\text{OUT}} = I_{\text{rms}}\left(1 - \frac{1}{16(1+4\omega^2\tau^2)}\right) + \frac{I_{\text{rms}}\sin(2\omega t)}{2\sqrt{1+4\omega^2\tau^2}} \tag{15}$$

$$\%\ \text{dc error} = \frac{1}{16(1+4\omega^2\tau^2)} \times 100\% \tag{16}$$

and the percent ripple is

$$\%\ \text{ripple} = \frac{1}{2\sqrt{1+4\omega^2\tau^2}} \times 100\% \tag{17}$$

In order to give a good performance in the required frequency range, the value of capacitor C_{AV} must be chosen such that [7]

$$C_{\text{AV}} \gg \frac{g_{\text{m6(max)}}}{4\pi f_{(\text{min})}}$$

or

$$C_{\text{AV}} \gg \frac{I_{\text{M}}}{4\pi V_{\text{T}} f_{(\text{min})}} \tag{18}$$

where $f_{(\text{min})}$ is the lowest frequency of the interested frequency range and V_{T} is the thermal voltage. The cut-off frequency of the averaging circuit is

$$f_{\text{c}} = \frac{I_{\text{M}}}{4\pi V_{\text{T}} C_{\text{AV}}} \tag{19}$$

Note that the frequency of the input current must not be less than f_{C} for decreasing the percent ripple. For example, if the amplitude of the sinusoidal input current $I_{\text{M}} = 1$ mA and the frequency range of 1 kHz to 1 MHz ($f_{(\text{min})} = 1$ kHz) are considered, the capacitor C_{AV} must be chosen to be greater than 3.06 μF. However, if we choose the capacitor C_{AV} of 10 μF, the lower cut-off frequency is about 306 Hz. Then, we can employ a C_{AV} of 10 μF. In this case, from Eqs. (16) and (17), the conversion errors that are determined at the frequency of 10 kHz, $I_{\text{M}} = 1$ mA and $C_{\text{AV}} = 10$ μF are: the percent dc error 5.85×10^{-3}% and the percent ripple error 1.53%. The errors can be further reduced if a larger capacitor is used, but it will result in a longer settling time. It should be noted that this large value of capacitance is not suitable for monolithic integration. To reduce the size of capacitor, a miller capacitor multiplier can be used [15].

The second factor that causes the error is the current reflection errors associated with the positive current mirrors which can be given by

$$\varepsilon_{\text{pos}} = \frac{2}{\beta_{\text{npn}}} \pm \left(\frac{\Delta V_{\text{BE}}}{V_{\text{T}}}\right)_{\text{npn}} \tag{20}$$

where $(\Delta V_{\text{BE}}/V_{\text{T}})$ npn refers to mismatching of npn transistors. Assuming that overall V_{BE} mismatching is of the order 0.25 mV and $\beta > 100$, these errors will be less than 2%. This error can be further reduced if Wilson current mirrors are employed. The dynamic range of the conversion circuit is determined by the dc bias current I_{B1}. At the translinear cell, since the base current of Q_1 is extracted from the bias current I_{B1}, the signal current I_{IN} will clamp if the base current attempts to exceed this level. Therefore, the circuit dynamic range is approximately equal to $|I_{\text{IN}}| < I_{\text{B1}}$. Concerning with the power supply voltage from Fig. 2, the circuit can

operate at a power supply voltage of $2\,V_{BE}+V_{CEsat} \approx 1.8\,V$. Thus, a minimum power supply voltage that the circuit can function properly is about 2 V.

3. Simulation and experimental results

The performances of the proposed rms-to-dc conversion circuit of Fig. 2 were demonstrated through the simulation results using PSPICE and also through the experimental results from the circuit constructed on prototype board. All the transistors and dc current sources were commercially available npn BJTs 2N3904 and three-terminal adjustable current sources LM334, respectively. The supply voltage and dc bias currents of the circuit are set to $+V_{CC} = +5\,V$ and $I_{B1} = I_{B2} = I_{B3} = I_{B4} = 1\,mA$, respectively. The performance of the circuit that is summarized from the experimental results is listed in Table 1, where the values of the currents I_{IN} and I_{rms} were measured from the voltage across the resistors of 1 kΩ. We found that the circuit exhibits a maximum nonlinearity of 0.1%, for input current with peak amplitude of 10 μA to 1 mA.

The high-frequency response cannot be measured directly from the bread-board circuit because of the stray capacitance in the circuit board and the finite bandwidth of the voltage-to-current converter. The PSPICE simulation program is used to analyze instead. The gain bandwidth product f_T of 2N3904 transistor is 350 MHz. The frequency response for the case of the sinusoidal input current with the amplitude of I_{IN} of 200 μA, 500 μA and 1 mA (100% of the maximum current) are illustrated in Fig. 3. The bandwidths are about 10, 30 and 60 MHz, respectively. It should be note that the g_{m6} are varied in direct proportion to the input current (I_{IN}). Therefore, if I_{IN} is increased, the cutoff frequency of the rms-to-dc converter is also increased. Table 2 is the summary of the simulation results for −3 dB bandwidth of the input current I_{IN} ranging from 10 μA to 1 mA.

Fig. 4 shows the experimental results to demonstrate the linearity of the rms-to-dc converter. The transfer characteristic shows the plot of the I_{rms} against the input signal current

Table 1. Experimental results for the performance of the circuit in Fig. 2

Power requirements	
Rated supply voltage	$+2\,V_{DC}$ to $+15\,V_{DC}$
Quiescent current (max)	1 mA
Input characteristic	
Input current range (max)	1 mA
Input resistance	≅15 Ω
Accuracy	
Conversion accuracy	0.1% max. nonlinearity, 10 μA to 1 mA input current
Crest factor	CF = 4, error 0.5% CF = 10, error 2.5%

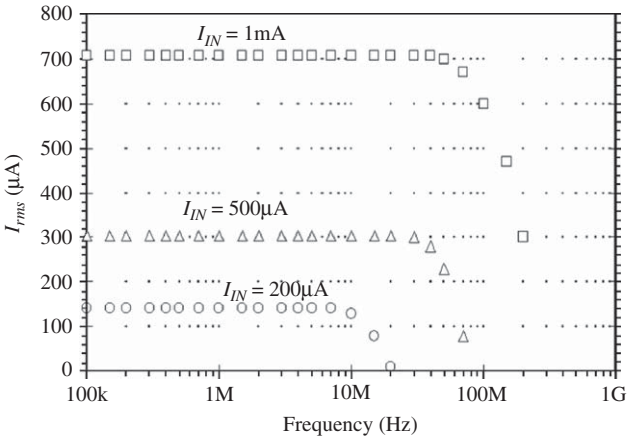

Fig. 3. High-frequency responses due to the various input current I_{IN}.

Table 2. High-frequency response simulation results for various signal levels of input current I_{IN} for the circuit in Fig. 2

Peak amplitude values	−3 dB bandwidth
$I_{IN} = 10\,\mu A$	700 kHz
$I_{IN} = 100\,\mu A$	5 MHz
$I_{IN} = 200\,\mu A$	10 MHz
$I_{IN} = 500\,\mu A$	30 MHz
$I_{IN} = 1\,mA$	60 MHz

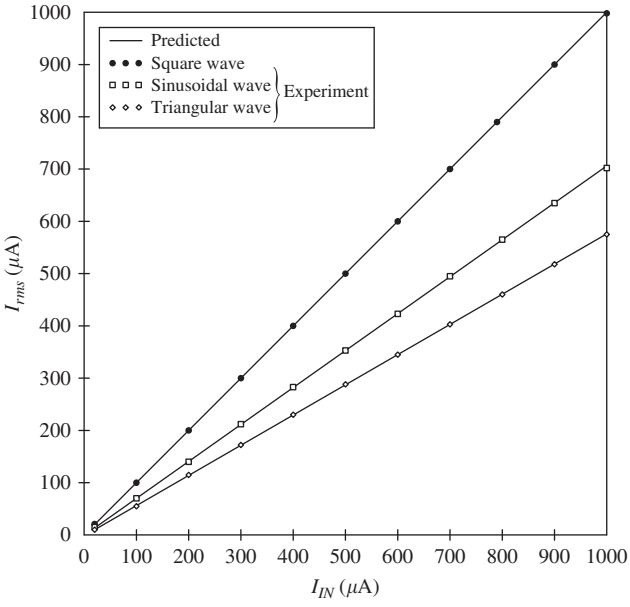

Fig. 4. The transfer characteristic of the I_{rms} against the input currents I_{IN}.

I_{IN} with the amplitude of 10 μA to 1 mA for the sine, triangular and square waveforms at $C_{AV} = 1\,\mu F$ and frequency input 10 kHz. We found that the maximum conversion

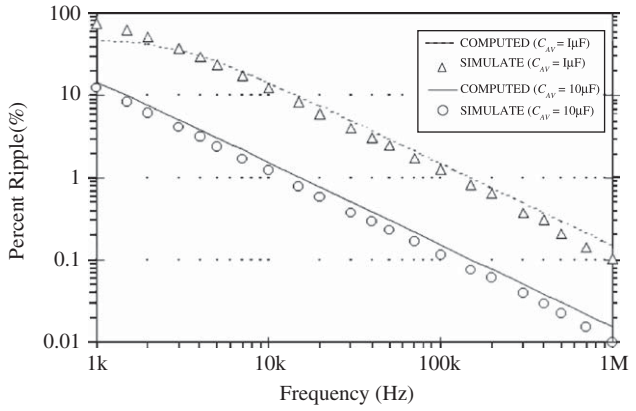

Fig. 5. The comparison between theoretical and simulation results of the percent ripple of the output current.

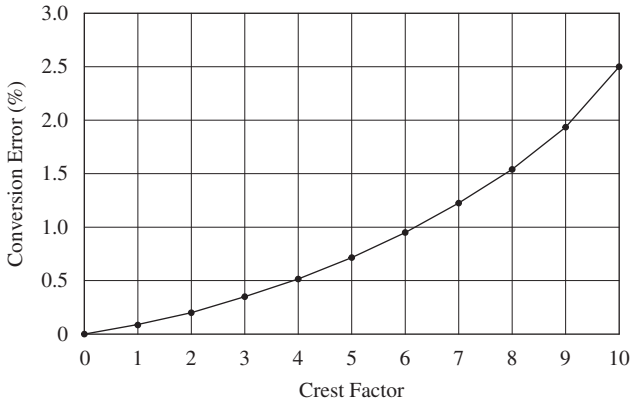

Fig. 6. Simulation results for the conversion error versus crest factor.

nonlinearity is about 0.1%. The results are in good agreement with the predicted value of Eq. (16). The percent ripples at the output for the value of averaging capacitor C_{AV} of 1 μF and 10 μF, which are computed from Eq. (17) and simulated by PSPICE, are plotted in Fig. 5. The input is the sine wave current with a amplitude of 1 mA and with frequency range 1 kHz to 1 MHz. For example, at the frequency of 10 kHz the percent ripples that are computed from Eq. (17), for $C_{AV} = 1$ μF and $C_{AV} = 10$ μF, are 15.3% and 1.53%, respectively, where the simulated percent ripples are 13% and 1.2%, respectively. Noting that, with the same capacitor, the values of the percent ripple can be further reduced if we increase the frequency of the signal.

The simulation results for the input signal with different crest factors are shown in Fig. 6. The plot shows the conversion error in the case of $I_{IN} = 1$ mA, with the crest factor varied from 1 to 10. The rectangular pulse train with pulse width of 100 μs was used for this test, since it is the worst-case waveform for rms measurement (all the energy is contained in the peak current I_M). The duty cycle and peak amplitude were adjusted to produce crest factors from 1 to 10, while maintaining a constant 1 mA input current. From the graph we can describe that the percent error is not greater than 2.5%.

4. Conclusion

A design of the translinear-based true rms-to-dc converter through the use of an explicit computation method has been proposed. The conversion circuit consists of the current-mode squarer, averaging and square root circuits. Since only npn bipolar junction transistors are used, the circuit can be operated at low supply voltage. As was summarized in Table 1, the simulation and experimental results have been used to display the performances of the proposed circuit.

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References

[1] Kolanko JK. Accurate measurement of power, energy, and true rms voltage using synchronous counting. IEEE Trans Instrum Meas 1993;42:752–4.
[2] Seevinck E, Wassenaar RF, Wong HCK. A wide-band technique for vector summation and rms-to-dc conversion. IEEE J Solid-State Circuits 1984;SC-19:311–8.
[3] Wassenaar RF, Seevinck E, Van Leeuwen MG, Speelman CJ, Holle E. New technique for high-frequency rms-to-dc conversion based-on a multifunctional v-to-i converter. IEEE J Solid-State Circuits 1988;23:802–14.
[4] Northrop RB. Analog electronic analysis and application. New York: Addison-Wesley; 1990.
[5] Mulder J, Serdijn WA, van derr Woerd AC, van Roermund AHM. Dynamic translinear rms-dc converter. Electron Lett 1996;32:2067–8.
[6] Mulder J, van der Woerd AC, Serdijn WA, van Roermund AHM. An rms-dc converter based on the dynamic translinear principle. IEEE Solid-State Circuits 1997;32:1146–50.
[7] Surakampontorn W, Kumwachara K. A dual translinear-based true rms-to-dc converter. IEEE Trans Instrum Meas 1999;47:456–64.
[8] Peyton AJ, Walsh V. Analog electronics with op amps. Cambridge: Cambridge University Presss; 1993.
[9] Kitckin C, Counts L. Rms to dc conversion application guide. Analog Device 1986.
[10] Gilbert B. Translinear circuit: a proposed classification. Electron Lett 1975;11:14–6.
[11] Toumazu C, Lidgey FT, Haigh DG. The current mode approach. London, UK: Peter Feregrinus; 1990.
[12] Seevinck E, Wiegerink RJ. Generalized translinear circuit principle. IEEE J Solid-State Circuits 1991;26:1098–102.

[13] Greeniech EW. Analog integrated circuits. New York: Chapman & Hall; 1997.
[14] Greeniech EW. Function circuits design and applications. New York: Burr-Brown Research Corporation; 1976.
[15] Rincon-Mora GA. Active capacitor multiplier in miller-compensated circuits. IEEE Int Symp Circuit Syst 2000;35: 26–32.

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