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Paper ID : 0030
Title : A Novel Widely Linear Current-Tunable CMOS Transconductor
Author(s) : Khanittha Kaewdang, Wanlop Surakampontorn

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Review Comments:

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Please check the directions of io and -io of Fig. 1 and Fig. 4. The performance of the power consumption and CMRR should be also indicated.

--- Comments from Reviewer #2 ---

Good simulation results are obtained.

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A Novel Widely Linear Current-Tunable CMOS Transconductor

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Abstract- **A CMOS-based linearly tunable transconductor is proposed in this paper. The realization technique is achieved by using a fully differential transconductor and a current variable gain stage, for a power supply of ±1.5V. Its transconductance gain can be linearly tuned by an external bias current for more than 4 decades. The transconductor cell is designed in 0.5μm AMIS technology. The performance of the proposed circuit is discussed and confirmed through PSPICE simulation results.**

I. Introduction

Transconductor circuits are the essential active building blocks of many analog applications such as amplifiers, multiplier, active filters and sinusoidal oscillators. Moreover, when the transconductance gain of the transconductor can be electronically and linearly varied, they can also be applied in automatic gain control circuits and in analog multipliers.

There have been several approaches of designing tunable linear CMOS transconductors, where those approaches are claimed to achieve the linear operation in the square law of the I-V characteristic of MOS transistors [1]-[4]. However, most of them are functioning in voltage controlled mode. Their controllable voltage ranges are rather limited and only narrow linearly transconductance ranges are available. In the past, a current controlled CMOS transconductor was presented in [5]. But the linear tunable transconductance range is narrow due to the MOS transistors are working in the weak-inversion region. On the other hand, an Electronically Tunable Operational Transconductance Amplifier (EOTA), where its g_m can be linearly tuned for a wide range, has been proposed [6]. However, its structure which composed of 3 OTAs is quite complicated. Therefore, the main objective of this paper is to propose the new technique to realize a wide linearly and electronically tuned CMOS transconductor. The realization is based on the used of a fully differential transconductor and a variable current gain cell that is constructed using a current mode translinear circuit. The proposed transconductor is suitable for integrated circuit form. In addition, the circuit characteristics are studied through PSPICE simulation results and the preliminary results for a new technique are reported.

II. Circuit Descriptions

In order to realize a CMOS transconductor with the transcondcuctance gain can be electronically and linearly tuned, in this work, a fully differential transconductor and the variable current gain cell is employed as active circuit elements. Since it is generally assume that all MOS transistors are operating in the saturation region, hence the individual functions of the circuits are derived from the approximate square-law characteristic of MOS transistors in saturation.

A. *Fully Balanced Differential Transconductor*

A fully balanced differential transconductor structure is shown in figure 1. Let M_1 and M_2 are perfectly matched, the current mirrors have unity current gains and all transistors are operated in saturation region. v_{in} is the differential input voltage ($v_{in}=v_1-v_2$), i_o and $-i_o$ are the output currents and I_B is the bias current. Its differential output current can be given by

$$i_o = -i_o = i_2 - i_1 = \frac{\mu_n C'_{ox}}{2}\left(\frac{W}{L}\right) v_{in}\sqrt{\frac{4I_B}{\mu_n C'_{ox}(W/L)} - v_{in}^2} \qquad (1)$$

and its transconductance gain (g_m) can be written as

$$g_m = \frac{i_o}{v_{in}} = \frac{\mu_n C'_{ox}}{2}\left(\frac{W}{L}\right)\sqrt{\frac{4I_B}{\mu_n C'_{ox}(W/L)} - v_{in}^2}\left[1 - \frac{v_{in}^2}{\frac{4I_B}{\mu_n C'_{ox}(W/L)} - v_{in}^2}\right] \qquad (2)$$

For the small signal of v_{in}, the transconductance gain of the fully differential transconductor can be derived by taking the derivative of (1) with respect to v_{in}, yielding

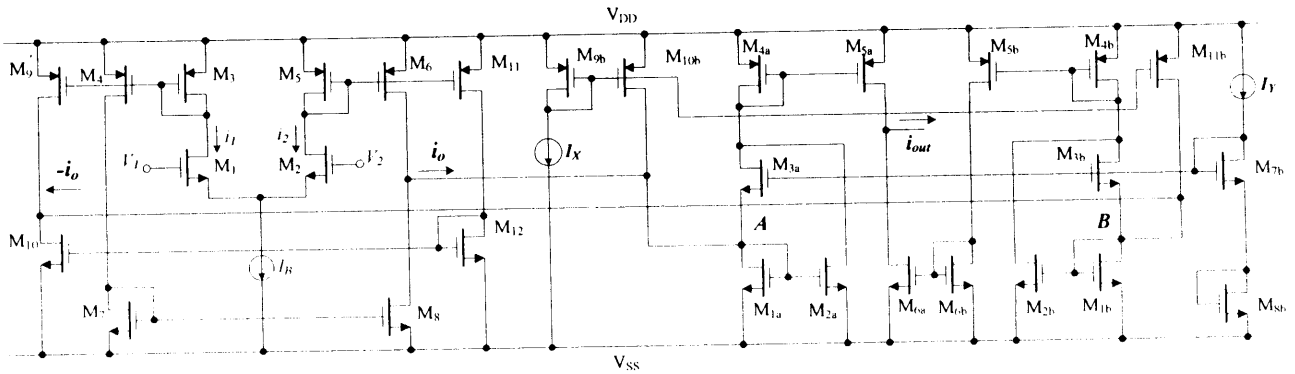

Fig. 4 Complete schematic diagram of the proposed transconductor

Figure 4 shows the complete schematic circuit diagram of the proposed CMOS-based transconductor. It consists of a transconductance cell in corporation with the variable current gain cell. However, to demonstrate the design concept, a transconductor cell in the form of a source-coupled pair differential amplifier is employed as basic circuit building block. The circuit is simple and suitable for implementing in integrated circuit form.

From routine circuit analysis the output current of the proposed circuit can be expressed as

$$i_{out} = A_C \cdot i_o \tag{10}$$

From equation (5) and (9) the output current of the proposed transconductor can be expressed as

$$i_{out} = \sqrt{2KI_B} \cdot \frac{nI_X}{2I_Y} \cdot v_{in} \tag{11}$$

It can be shown that

$$G_m = \frac{n\sqrt{2KI_B}}{2I_Y} I_X = K_T I_X \tag{12}$$

where $K_T = n\sqrt{2KI_B}/2I_Y$, which can usually be kept to constant. The equation (12) clearly indicate that the transconductance gain of the proposed transconductor can be electronically and linearly tuned by the bias current I_X. Since the current $|I_x|+|i_{in}|$ should be limited to be less than $4I_Y$, therefore, for a wide current tunable range, the bias current I_Y should be a high constant current. It worth noting that the input dynamic and nonlinearity range is not affected by the adjustment of I_X.

III. Simulation Results

The performance of the proposed transconductor is verified through the PSPICE simulation. All the CMOS transistor is simulated by using CMOS transistor parameters of the AMIS technology 0.5μm of MOSIS with V_{tn} = 0.67V and V_{tp}= -0.91V. For the proposed circuit in Fig. 4, by setting n=2 and the dimensions of all CMOS transistors are listed in Table I. The power supply voltages are set to V_{DD} = -V_{SS} = 1.5V.

TABLE I
THE TRANSISTOR DIMENSIONS

MOSFETs	W(μm)	L(μm)
M_1-M_{12}, M_{1a}- M_{4a} ,M_{6a}, M_{1b}-M_{4b}, M_{6b}-M_{11b}	5	0.5
M_{5a},M_{5b}	10	0.5

Figure 5 shows the simulated transfer characteristic of the proposed transconductor. The plots of the output current i_{out} versus the input voltage v_{in} for the controlled current (I_X) in the cases of 600μA, 800μA and 1mA for I_B and I_Y were set to 100μA and 400μA, respectively. These results show that the transconductor can linearly convert the input voltage into output signal current with nonlinearity of less than 4% for the input voltage (v_{in}) in the ranges of -200mV to 200mV. The results were agreed with the prediction value from Eq. (12). For example, in the case of the DC bias current I_X = 1mA, I_B=100 μA, I_Y=400 μA and V_{in}=0.2V the transconductance gain G_m =8.5×10^{-4} A/V, for $\mu_n C_{ox}/2$ =5.78×10^{-5} A/V^2 and W/L =10.

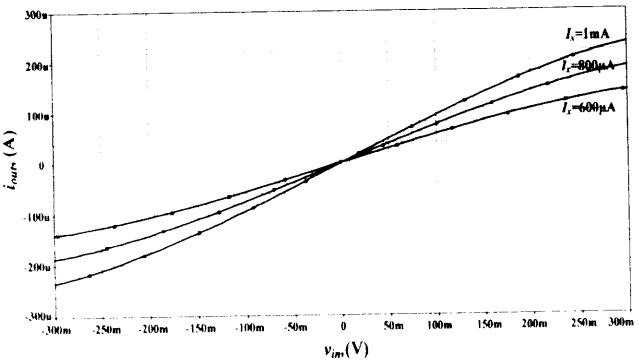

Fig. 5 DC transfer characteristics

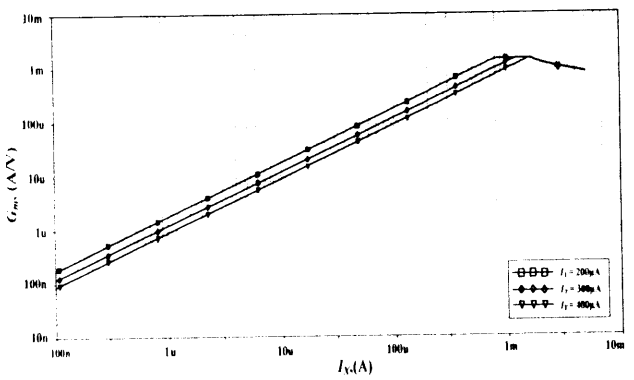

Fig. 6 Transconductance gain linearly tuned range

The plot of the relation between the transconductance gain G_m and the bias current I_X in the figure 6 is measured by fixing V_{in} = 0.2V, I_B=100 μA and in the case of I_Y=200 μA, 300 μA and 400 μA respectively, by varying I_X from 100nA to 5mA. It shows that the transconductance gain G_m can be linearly tuned by the bias current I_X over the range of 100nA to 1.6mA, where the simulated conversion errors are less than 3.7%. It can be clearly seen that the transfer characteristic demonstrated that the simulated and calculated data are in a good agreement and its transconductance gain can be linearly and electronically tuned for a wide range. Noting for the case of I_Y=200 μA, I_Y=300 μA and I_Y =400 μA, the tunable range are limited by about $I_X \approx$ 8mA, $I_X \approx$ 1.2mA and $I_X \approx$ 1.6mA, respectively. This confirm the condition that the current $|I_X|+|i_{in}|$ should be less than $|4I_1|$.

The achieved THD of the output current is less than 1.4% for an input sinusoid with 200mV peak value and 50MHz frequency. The total power consumption is 20mW with ±1.5V supply voltage in typical situation. In addition, the CMRR of the proposed transconductor is depended on the differential CMOS OTA, CMRR = $2g_{m1}R_Bg_{m3}(r_{o6}/r_{o8})$ [8]. From the simulation result, by replacing the ideal current source the CMRR is about 90dB.

In figure 7, the frequency response of the transconductor is also studied, where the -3 dB bandwidth of about 780 MHz is achieved.

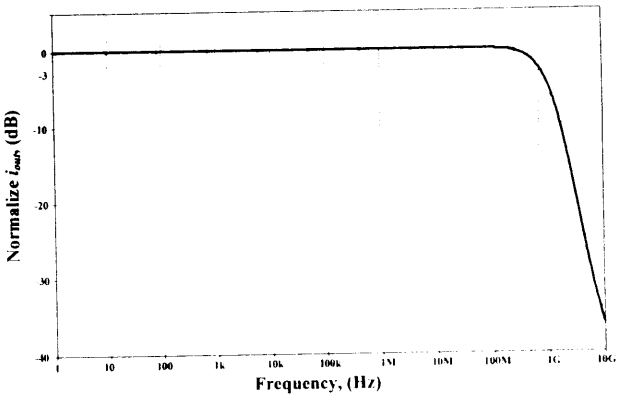

Fig. 7 The frequency response of the proposed transconductor

IV. Conclusions

The circuit technique to realize an electronically and linearly tunable range CMOS transconductor with wide tunable range has been proposed. The realization scheme is suitable for implemented in a standard CMOS process. Its transconductance gain can be electrically and linearly tuned by the external DC bias current in the range of about 100nA to 1.6mA, where the transconductor's nonlinearity is less than 3.7%. The simulation indicates a -3dB bandwidth of about 780MHz. Simulation results ensure our proposed technique and demonstrate the performances of the proposed circuit.

Acknowledgment

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References

[1] E. Klumperink, Zwan and E. v.d. "CMOS variable transconductance circuit with constant bandwidth" Electronics Letters, vol. 25, 1989. pp. 675-676.

[2] S.-C. Huang, M. Ismail, "Linear tunable COMFET transconductor," Electronics Letters, vol. 29, no. 5, 1993. pp 459-461.

[3] Z. Wang and W. Guggenbuhl "A voltage-controllable linear MOS transconductor using bias offset technique," IEEE Solid-State Circuits, vol. 25, 1990. pp.315 - 317.

[4] G. Wilson and P.K. Chan "Saturation-mode CMOS transconductor with enhanced tunability and Low distortion," Electronics Letters, vol. 29, 1993. pp.459-461.

[5] C.-C. Hung, and K. Halonen "Micropower CMOS GM-C filters for speech signal processing," IEEE International Symposium on Circuit and systems , 1997. pp. 1972-1974.

[6] K. Kaewdang, and W. Surakampontorn, "On the realization of electronically current-tunable CMOS OTA," International Journal of Electronics and Communications, International Journal of Electronics and Communications, vol. 61, Issue 5,May 2007, pp. 300-306.

[7] W. Surakampontorn and K. Kumwachara, "CMOS-based electronically tunable current conveyor," Electronics Letters, vol. 28, no.14,1992. pp. 1316-1317.

[8] Kenneth R. Laker and Willy M.C. Sansen, Design of analog and integrated. New York, McGraw-Hill, 1994.

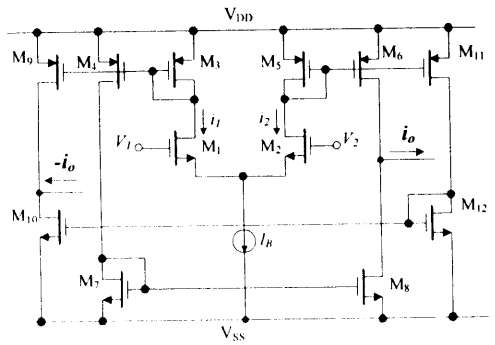

Fig. 1 CMOS differential transconductor

$$\left.\frac{di_o}{dv_{in}}\right|_{v_{in}=0} = \sqrt{\mu_n C_{ox}(W/L) I_B} \qquad (3)$$

therefore, the transconductance gain can be defined as

$$g_m = \sqrt{2KI_B} \qquad , \quad -\sqrt{\frac{I_B}{K}} \le v_{in} \le \sqrt{\frac{I_B}{K}} \qquad (4)$$

where $K = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)$ is the transconductance parameter, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length. Thus we can obtain the following equation for a small signal:

$$i_o = g_m v_{in} = \sqrt{2I_B K}\cdot v_{in} \qquad (5)$$

Equation (4) shows that the transconductance gain (g_m) of the OTA can be varied by the bias current I_B, but in the form of a square root function. It should be noted that the transconductance gain (g_m) of the transconductor shown in figure 1 will provide low harmonic distortion if the input voltage is limited in the range of

$$-\sqrt{\frac{I_B}{K}} \le v_{in} \le \sqrt{\frac{I_B}{K}} \qquad (6)$$

B. Variable Current Gain Cell

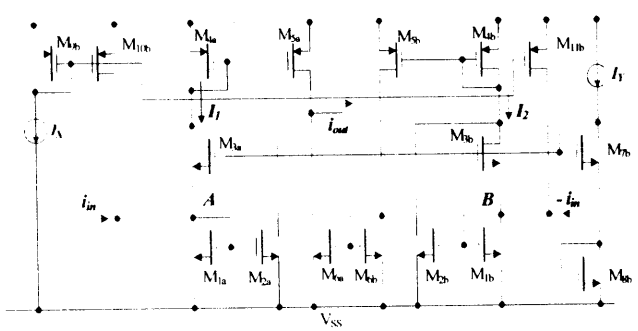

Fig.2 Variable current gain cell

Let us consider the schematic diagram shown in Fig.2, where the operation of the circuit is based on the square law characteristic of MOS transistors biased in the saturation region. Transistors M_{1a} through M_{3a} and transistors M_{1b} through M_{3b} function as the current squarer, whereas transistors M_{8b} and M_{9b} and the current source I_Y formed as the current-controlled bias circuit. The current mirrors M_{4a}-M_{5a} and M_{4b}-M_{5b} have current gain ratios equal to 1: n. The input signal current i_{in} and $-i_{in}$ are injected into point A and B respectively where the input signal are added with the DC current (I_X) that form by the current source I_X and the unity gain current mirror (M_{10b} through M_{12b}). Therefore the differential input currents that flow into point A and B are $I_X + i_{in}$ and $I_X - i_{in}$ respectively. By using the square law of MOS transistors operating in the saturation region, the current I_1 and I_2 can be given by [6]

$$I_1 = 2I_1 + \frac{(I_X + i_{in})^2}{8I_1} \quad , \quad I_2 = 2I_1 + \frac{(I_X - i_{in})^2}{8I_1}$$

and the output current of the current gain cell can be expressed as

$$i_{out} = n(I_1 - I_2) = (nI_X/2I_1)i_{in} \text{ , for } |I_X| + |i_{in}| \le 4I_1 \qquad (7)$$

or $$i_{out} = (nI_X/2I_1)i_{in} = A_C\, i_{in} \qquad (8)$$

where A_C is the current gain of the variable current cell and can be expressed as

$$A_C = nI_X/2I_1 \qquad (9)$$

We can see that the output current can be tuned by the DC bias current I_X and I_1. This indicates the gain is proportional to I_X and I_1.

C. Complete Widely Linear Current-Tunable Transconductor

The overall block diagram of the linear tunable transconductor circuit is shown in Fig. 3. It consists of the fully balanced differential transconductor cascaded with the variable current gain cell.

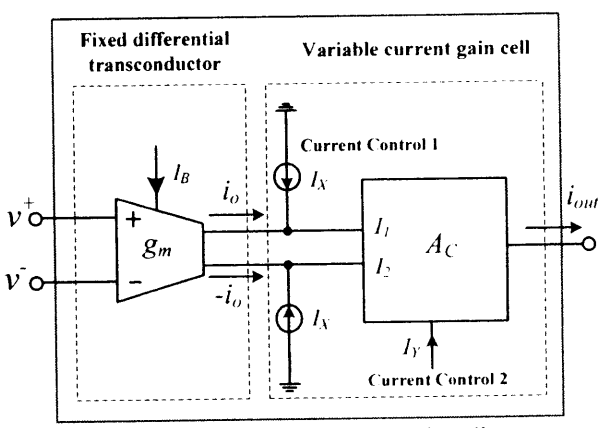

Fig. 3 Building block of the proposed widely linear current-tunable CMOS transconductor

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