On the realization of electronically current-tunable CMOS OTA

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Abstract

A CMOS operational transconductance amplifier (OTA) called as an EOTA, where its transconductance gain can be electronically and linearly tuned is proposed in this paper. The realization method is achieved by squaring the transconductance gain of the balanced CMOS OTA. The EOTA transconductance gain can be linearly tuned by an external bias current for three decades. The linear input-voltage range of about 1Vp with less than 1% nonlinearity is obtained. The usefulness of the proposed EOTA is demonstrated through application example with a current multiplier. The performance of the proposed circuit is discussed and confirmed through PSPICE-simulation results.

1. Introduction

Linear transconductors or voltage-to-current converter circuits are fundamental building blocks of analog circuits and systems. They are found useful in interface circuits, instrumentation amplifiers, continuous-time-filters and oscillators. In addition, when the transconductance gain of the transistor can be electronically varied, they can also be applied in automatic gain control circuits and in analog multipliers. In the last two decades, it is well accepted that a linear transconductor, which is constructed from a bi-polar differential pair and current mirrors, called as an operational transconductance amplifier (OTA), is one of the essential active building blocks in the design of analog circuits [1–3]. This is due to the fact that the OTA is a low-cost device that has only a single high-impedance node and its transconductance gain \( g_m \) can be linearly controlled over more than four decades by means of an external bias current. Moreover, the implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplified the design.

In CMOS technology, several linearly tunable transconductors based on the use of MOS transistors operating in saturation region have been proposed in the literature [4–7]. Most of them are functioning in voltage-controlled mode. The method of source-follower of Ref. [4] is operated in square law characteristic with constant source-bulk voltages, where the control voltage is applied to the gate. Whereas for the cross-coupled connection methods [5–7], the transconductance control voltages are applied through voltage-level shifters. However, their controllable voltage ranges are rather limited and only narrow linearly tunable transconductance ranges are available. In some applications, such as, an analog multiplier circuit, a frequency divider/multiplier circuit and an arbitrary power-law circuit, current-controlled transconductors that this transconductance gain can be linearly controllable by a DC bias current are preferable [8–10]. In the past, a current-controlled CMOS transconductor was...
presented in Ref. [11]. But the linearly tunable transconductance range is narrow due to the MOS transistors are working in the weak-inversion region.

The main objective of this paper is, therefore, to present a circuit design technique for the synthesis of a linear electronically tunable CMOS OTA, called as an EOTA. Since, the realization method is achieved by squaring the transconductance gain of the CMOS OTA, the transconductance gain of the EOTA is directly depend on the DC bias current. To provide a maximum output voltage swing and wide linearly tunable transconductance range, a balanced CMOS OTA or voltage-to-current transducer will be employed as basic active circuit elements to realize the EOTA, whereas the completed EOTA requires three balanced CMOS OTA’s. Since it is generally assumed that all MOS transistors are operating in the saturation region, the individual functions of the circuits are derived from the approximate square-law characteristic of MOS transistors in saturation. In addition, it is well accepted that all MOS devices operate in the saturation region. This means that the transistor drain current $I_D$ is characterized by a square-law model as

$$ I_D = K(V_{GS} - V_T)^2 \quad \text{for} \quad V_{GS} > V_T, $$

$$ = 0 \quad \text{for} \quad V_{GS} \leq V_T, $$

(1)

where the transconductance parameter $K = \mu C_{ox} W/2L$, $\mu$ is the mobility of the carrier, $C_{ox}$ is the gate-oxide capacitance per unit area, $W$ is the effective channel width, $L$ is the effective channel length, and $V_{GS}$ and $V_T$ are the gate-to-source and the threshold voltages, respectively.

2. Circuit description

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. This means that the transistor drain current $I_D$ is characterized by a square-law model as

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2.1. A balanced CMOS OTA

Fig. 1 shows a balanced single-output CMOS OTA, which is formed by MOS coupled pair and current mirrors, where $V_{in}$ is the differential input voltage ($V_{in} = V_1 - V_2$), $i_o$ is the output current and $I_{BB}$ is the bias current. Let us assume that $M_1$ and $M_2$ are perfectly matched and the current mirrors have unity current gain. By using Eq. (1), the differential output current of the circuit in Fig. 1 can be given by [12]

$$ i_o = i_2 - i_1 $$

\begin{align*}
&= \sqrt{2I_{BB}K}V_{in}\sqrt{1 - \frac{KV_{in}^2}{2I_{BB}}} \quad \text{for} \\
&- \sqrt{\frac{I_{BB}}{K}} \leq V_{in} \leq \sqrt{\frac{I_{BB}}{K}}. \\
(2)
\end{align*}

The transconductance gain ($g_m$) of the fully differential OTA can be derived by taking the derivative of Eq. (2) with respect to $V_{in}$, yielding

$$ g_m = \frac{d}{dV_{in}} \bigg|_{V_{in}=0} i_o $$

\begin{align*}
&= \sqrt{2I_{BB}K} \quad \text{for} \\
&- \sqrt{\frac{I_{BB}}{K}} \leq V_{in} \leq \sqrt{\frac{I_{BB}}{K}}. \\
(3)
\end{align*}

From Eq. (3) shows that the transconductance gain ($g_m$) of the OTA can be varied by the bias current $I_{BB}$, but in the form of square root function. In addition, in order to operate in the low distortion range, where all the transistors are operated in saturation, the input voltage $V_{in}$ should be in the range of [13]

$$ V_{in} \leq \sqrt{I_{BB}/K}. $$

(5)

2.2. The proposed electronically and linearly tunable CMOS OTA

Through the use of three balanced single-output CMOS OTAs, a CMOS-based electronically and linearly tunable OTA, called as an EOTA, can be realized by the circuit diagram shown in Fig. 2. The OTA1 converts a differential input signal voltage $v_{in} = v_1 - v_2$ into a signal current $i_L$ to
flow into an active resistor \( R_L \), formed by the OTA2, where \( Z_L = 1/g_{m2} \) and \( g_{m2} \) represents the transconductance gain of the OTA2. Since the current signal \( i_L = g_{m1}v_{in} \), the voltage drop across the active resistor (OTA2) becomes

\[
v_L = i_L Z_L = g_{m1}v_{in} \frac{1}{g_{m2}}.
\]

The OTA3 will convert the voltage \( v_L \), with the transconductance gain of \( g_{m3} \), into the output current \( i_{out} \) as

\[
i_{out} = g_{m3}v_L = g_{m1}v_{in} \frac{1}{g_{m2}}.
\]

From Eqs. (6) and (7), the current \( i_{out} \) can be rewritten as

\[
i_{out} = g_{m1}g_{m3}v_{in} \frac{1}{g_{m2}}.
\]

Since \( g_{m1} = \sqrt{2I_{BB1}K_1} \), \( g_{m2} = \sqrt{2I_{BB2}K_2} \) and \( g_{m3} = \sqrt{2I_{BB3}K_3} \), if we set \( I_{BB1} = I_{BB3} = I_{BE} \), then from Eq. (8), we obtain

\[
i_{out}^2 = \frac{2I_{BE}K_1K_3}{2I_{BB2}K_2} v_{in}^2 = g_{mT}v_{in}^2.
\]

where \( g_{mT} \) represents the transconductance gain of the proposed EOTA and can be expressed as

\[
g_{mT} = 2I_{BE}K_T
\]

and \( K_T = \sqrt{K_1K_3/2I_{BB2}K_2} \), which can usually be kept at constant. Eq. (10) clearly indicated that the transconductance gain of the proposed EOTA can be electronically and linearly tuned by the bias current \( I_{BE} \). This linear relationship is in the form that similar to the transconductance gain of the bi-polar-based OTA that found useful in many applications [14]. Since the balanced CMOS OTA is formed by MOS coupled pair and current mirrors, therefore, the proposed EOTA is very suitable for fabricating in CMOS integrated form.

3. Performance of the EOTA

It is well accepted that the prediction of Eq. (10) will be valid only for a small value of \( V_{in} \). From Eq. (5), since OTA1 and OTA3 are formed by MOS coupled pairs, to maintain in the linear range and low total harmonic distortion, the voltages \( V_{in} \) and \( V_L \) should, respectively, be restricted to the ranges of [13]

\[
|V_{in}|_{MAX} = 0.4/\sqrt{K} Z_L
\]

and

\[
|V_{in}|_{MAX} = 0.4\frac{I_{BE}}{I_{BB}}K.
\]

where it should be noted from Eq. (11) that the maximum usable voltage range is limited by \( |V_{in}|_{MAX} \) if \( g_{m1}/g_{m2} > 1 \) and it is limited by \( |V_{in}|_{MAX} \) if \( g_{m1}/g_{m2} < 1 \). For example, for \( I_{BE} = 1 \) mA and \( I_{BB2} = 700 \) mA, the maximum usable range is determined by \( |V_{in}|_{MAX} \) and \( |V_{in}|_{MAX} \) is about 0.94 V, for \( K = \mu_nC_{ox}W/2L = 1.27 \times 10^{-4} A/V^2 \), \( \mu_nC_{ox} = 5.08 \times 10^{-5} V \) and \( W/2L = 2.5 \).

The transconductance gain error that results from in the inaccuracy of the EOTA can be determined from a large signal analysis. Consider the balanced CMOS OTA, the transconductance gain \( G_m \) of the Eq. (2) can be written as

\[
G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_{BB}K} \left( 1 - \frac{K V_{in}^2}{2I_{BB}} \right) \text{ for } -\frac{1}{K} \leq V_{in} \leq \frac{1}{K}.
\]

If we set the transconductance error of the balanced CMOS OTA of Fig. 1 as \( E = KV_{in}^2/2I_{BB} \), then Eq. (12) can be rewritten as

\[
G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_{BB}K} \sqrt{1 - E}.
\]

We found that the \( G_m \) will equal to the \( g_m \) of Eq. (3) in the condition that \( KV_{in}^2/2I_{BB} < 1 \). This can be achieved by keeping the input voltage signal \( V_{in} \) small or set the DC bias current \( I_{BB} \) to a large value.

By applying the \( G_m \) of Eq. (13) to the circuit of Fig. 2, we obtain the transconductance gain of the proposed EOTA for large signal as

\[
G_m = 2I_{BB}K_T \left( 1 + \frac{\sqrt{1 - E_1} \sqrt{1 - E_3} - \sqrt{1 - E_2}}{\sqrt{1 - E_3}} \right),
\]

where the errors \( E_1 = K_1V_{in1}^2/2I_{BB1} \), \( E_2 = K_2V_{in2}^2/2I_{BB2} \) and \( E_3 = K_3V_{in3}^2/2I_{BB3} \) are the transconductance errors due to the OTA1, OTA2 and OTA3, respectively. Given that \( E_T \) is the transconductance error of the EOTA from the linear transconductance gain, we can write

\[
E_T = \frac{\sqrt{1 - E_1} \sqrt{1 - E_3} - \sqrt{1 - E_2}}{\sqrt{1 - E_2}}\times 100%.
\]

Thus, we have the percent of the conversion error as

\[
\% E_T = \frac{\sqrt{1 - E_1} \sqrt{1 - E_3} - \sqrt{1 - E_2}}{\sqrt{1 - E_2}}\times 100%.
\]
For example, if $V_{in1} = 0.5 \, \text{V}$, $V_{in2} = V_{in3} = 0.751 \, \text{V}$, $I_{BB1} = I_{BB3} = I_{BE} = 1 \, \text{mA}$, $I_{BB2} = 700 \, \mu\text{A}$ and $K_1 = K_2 = K_3 = 1.27 \times 10^{-4} \, \text{A/V}^2$, the resulting transconductance error (% $E_T$) is equal to 0.54%.

### 4. A current multiplier circuit

In order to demonstrate the applications and the usefulness of the proposed EOTA, an application example will be outlined in this section. It outlines the use of the EOTA to realize the current-mode multiplier which employs only active circuit elements.

The current multiplier circuit is shown in Fig. 3. This application is adapted from the bipolar-based OTA-based circuits by replacing the bipolar-based OTA with the proposed EOTA [15]. From the figure, the input signal current $i_{in}$ is injected into the EOTA1, which is connected as a current-controlled grounded resistor. The voltage across the EOTA1 is then used as the input voltage for the EOTA2 and EOTA3. The input signal current $i_{in1}$ is added with the bias current $I_{BE2}$ of the EOTA2. Let $g_{mT1}$, $g_{mT2}$ and $g_{mT3}$ be the transconductance gains of the EOTA1, EOTA2 and EOTA3, respectively. Then from Eq. (9) and from routine circuit analysis the output currents $i_{o2}$ and $i_{o3}$ of the EOTA2 and EOTA3, respectively, can be written as

$$i_{o2} = \frac{g_{mT2}}{g_{mT1}} i_{in1} = \frac{(I_{BE2} + i_{in2})}{I_{BE1}} i_{in1}$$

and

$$i_{o3} = -\frac{g_{mT3}}{g_{mT1}} i_{in1} = -\frac{I_{BE3}}{I_{BE1}} i_{in1},$$

where $I_{BE1}$, $I_{BE2}$ and $I_{BE3}$ represent the DC bias current of the EOTA1, EOTA2 and EOTA3, respectively, and the transconductance gains $g_{mT1} = 2I_{BE1}K_1$, $g_{mT2} = 2(I_{BE2} + i_{in2})K_2$ and $g_{mT3} = 2I_{BE3}K_3$. If we set $I_{BE2} = I_{BE3} = I_{B}$, the output current $I_{out}$ of the circuit that is the summation of the currents $i_{o2}$ and $i_{o3}$ can be expressed as

$$I_{out} = i_{o2} + i_{o3} = \frac{i_{in1}i_{in2}}{I_{BE1}},$$

which is in the form of a current multiplication function.

### 5. Simulation results

The performance of the proposed EOTA of Fig. 2 and its applications were verified through the use of PSPICE-simulation results. All the balanced CMOS OTA was simulated using CMOS transistor parameters of the SC2N level 2 of MOSIS [16]. The dimensions of transistors $M_1$ and $M_2$ are $W = 50 \, \mu\text{m}$ and $L = 10 \, \mu\text{m}$, the dimensions of the transistor $M_3$ and $M_8$ are $W = 100 \, \mu\text{m}$ and $L = 10 \, \mu\text{m}$. The power supply voltage were set to $V_{DD} = -V_{SS} = \pm 5 \, \text{V}$. Fig. 4 shows the simulated transfer characteristic of the EOTA of Fig. 2. The plots of the output current $I_{out}$ versus the input voltage $V_{in}$ show that, for the DC bias current $I_{BE}$ in the cases of 1 mA, 800 mA and 400 mA, the EOTA can linearly convert the input voltage into output signal current with nonlinearity of less than 1% for the input voltage ($V_{in}$) in the ranges of $-1$ to $1 \, \text{V}$, $-0.86$ to $0.86 \, \text{V}$ and $-0.66$ to $0.66 \, \text{V}$, respectively. These results were agreed with the prediction value from Eq. (9). For example, for the case of the DC bias current $I_{BE} = 1 \, \text{mA}$ and for $V_{in} = 0.86 \, \text{V}$, $I_{BB2} = 700 \, \mu\text{A}$, the transconductance gain $g_{mT} = 5.398 \times 10^{-4} \, \text{A/V}$, where the conversion error is about 0.5%. The frequency response of the EOTA was also studied, where the $-3 \, \text{dB}$ bandwidth of about $120 \, \text{MHz}$ is achieved.

The plot of the relation between the transconductance gain $g_{mT}$ and the bias current $I_{BE}$ in Fig. 5 is measured by fixing $V_{in} = 0.1 \, \text{V}$ and varying $I_{BE}$ from 10 mA to 1 mA. It shows that the transconductance gain $g_{mT}$ can be linearly tuned by the bias current $I_{BE}$ over the range of $1 \, \mu\text{A}$ to $1 \, \text{mA}$ (three decades), where the simulated conversion error found to be about 0.68%. The similar relation of $g_{mT}$ versus $I_{BE}$ are also obtained for the cases of fixing $V_{in} = 0.2 \, \text{V}$ and $V_{in} = 0.5 \, \text{V}$. But in these cases the linear tunable ranges should be started at the current $I_{BE}$ that must more than 5 and 32 $\mu\text{A}$, respectively, since the entire MOS transistors must be operated in saturation region.

To demonstrate that the circuit of Fig. 3 can be functioned as current multiplier, two sinusoidal current signals are applied. Fig. 6 shows the response for the case of $i_{in1} = 0.2 \sin(2\pi10000\pi t) \, \text{mA}$, $i_{in2} = 0.2 \sin(2\pi20000\pi t) \, \text{mA}$ and $I_{B1} = 1 \, \text{mA}$. This result confirms that the circuit can accurately modulate two different input signal currents. The DC transfer characteristics of the multiplier circuit shown in Fig. 7 were observed by setting the bias currents $I_{B1} = I_{B2} = I_{B3} = 1 \, \text{mA}$, and the input current $i_{in1}$ and $i_{in2}$ are varied from $-200 \, \mu\text{A}$ to $200 \, \mu\text{A}$ with $100 \, \mu\text{A}$ per step. The transfer characteristic demonstrated that the simulated and calculated data are agreed very well over the input range of...
**Fig. 4.** DC transfer characteristics of the EOTA.

**Fig. 5.** Linear transconductance tunable range.

**Fig. 6.** Simulated transient response of the multiplier circuit.
190 µA with the error of less than 1%. The high-frequency characteristic of the multiplier circuit is also studied. The simulated −3 dB bandwidth for the case of the input \( i_{in1} \) to the output \( I_{out} \), with \( i_{in1} = 0.5 \sin(2\pi10000t) \) mA, \( i_{in2} = 500 \) µA and \( I_{B1} = 1 \) mA, is about 75 MHz and the simulated −3 dB bandwidth of the circuit for the input \( i_{in2} \) to the output \( I_{out} \), with \( i_{in2} = 0.5 \sin(2\pi10000t) \) mA, \( i_{in1} = 500 \) µA and \( I_{B1} = 1 \) mA, is about 71 MHz.

6. Conclusion

A design of the CMOS-based electronically and linearly current-tunable OTA has been proposed. The EOTA circuit composed of three balanced CMOS OTAs which is suitable for implementing in CMOS integrated form. The achieve characteristics of the proposed circuit were similar as the bipolar OTA that the transconductance gain (\( g_m \)) can be linearly tuned by the DC bias current. Simulation results have been employed to demonstrate the performances of the proposed EOTA. Moreover to confirm that EOTA can be replacing the bipolar OTA, the current-mode multiplier circuit is used to display the performances of the proposed circuit.

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References


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